Please amend the claims as follows:

1(Currently amended). A stack having a stack depth configured in a nonvolatile memory to store parameter values, where each memory write invalidates previous data.

2(Original). The stack of claim 1 wherein the nonvolatile memory includes a pair of blocks that are erased independently.

3(Original). The stack of claim 2 wherein valid parameter values are stored in a first block of the pair of blocks and a second block is erased.

4(Original). The stack of claim 3 wherein valid parameter values are stored in the second block of the pair of blocks and the first block is erased.

5(Original). The stack of claim 1 further including a register to store an offset value used to generate an address for words in the nonvolatile memory.

6(Original). The stack of claim 1 further including a smart stack controller to dynamically determine a number of blocks used in the stack.

7(Original). The stack of claim 1 further including a smart stack controller to distribute write cycles across multiple blocks of the nonvolatile memory.

8-10(Canceled).

11(Currently amended). A nonvolatile stack to store parameter values in words of a nonvolatile memory where a write of the nonvolatile stack invalidates previous instructions or data stored in the nonvolatile stack.

12(Currently amended). The nonvolatile stack of claim 11, wherein a memory pool in at least first and second blocks of the nonvolatile memory are sized to balance cycling and data retention capabilities with a write specification.

13(Currently amended). The nonvolatile stack of claim 11, further including a stack controller to distribute write cycles across multiple blocks of the nonvolatile memory.

14(Currently amended). The nonvolatile stack of claim 11, wherein the nonvolatile memory maps a received address to determine memory blocks to be written.

15(Currently amended). A storage device, comprising:

a nonvolatile memory having multiple blocks in a dynamic block swapped architecture, wherein a pair of blocks are configured to provide a first stack that stores ~~parameter values~~ data and instructions.

16(Original). The storage device of claim 15 further including a smart stack controller to distribute write cycles across the multiple blocks.

17(Original). The storage device of claim 15 further including a smart stack controller to dynamically determine which blocks from the multiple blocks are used in the first stack.

18(Original). The storage device of claim 15 wherein a second pair of blocks are instantiated in the storage device to configure a second stack.

19(Original). The storage device of claim 15 wherein multiple stacks are instantiated in the storage device with two blocks shared among the multiple stacks.

20(Currently amended). A computer system, comprising:
first and second antennas;
a transceiver coupled to the first and second antennas;
a processor coupled to the transceiver; and
a nonvolatile memory coupled to the processor to provide a nonvolatile stack to store parameter values that include both data and instructions.

21(Original). The computer system of claim 20 wherein the nonvolatile memory includes first and second blocks that are configured to form the nonvolatile stack and are erased independently.

22(Original). The computer system of claim 20 further including a register to store an offset value used to generate an address for words in the nonvolatile memory.

23-31(Canceled).